Debugging Techniques Using the Vivado Logic Analyzer

FPGA 2

Course Specification

- Instantiating the Debug Cores – HDL Instantiation Flow
- Lab 2: Adding a Debug Core Using the HDL Instantiation Flow
- Debug Flow in IP Integrator
- Lab 3: Debugging Flow – IPI Block Design
- Triggering and Visualizing Data
- Demo: Using Dashboards in the Vivado Logic Analyzer
- Demo: Trigger on Startup
- Tips and Tricks
- Lab 4: Tips and Tricks
- Scripting
- Lab 5: VIO Tcl Scripting
- Remote Access
- Lab 6: Remote Access (Optional)*

* Check with your Authorized Training Provider to confirm whether this content is included with your specific class.

Lab Descriptions

- Lab 1: Inserting a Debug Core Using the Netlist Insertion flow – Insert ILA cores into an existing synthesized netlist and debug a common problem.
- Lab 2: Adding a Debug Core Using the HDL Instantiation flow – Build upon a provided design to create and instantiate a VIO core and observe its behavior using the Vivado logic analyzer.
- Lab 3: Debugging Flow – IPI Block Design – Add an ILA IP core to a provided block design and connect nets to the core. Observe its behavior using the Vivado logic analyzer.
- Lab 4: Tips and Tricks – Sample across multiple time domains and use advanced trigger and capture capabilities.
- Lab 5: VIO Tcl Scripting - Configure automated analysis.
- Lab 6: Remote Access – Use the Vivado logic analyzer to configure an FPGA, set up triggering, and view the sampled data from a remote location.

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