Vivado Design Suite Static Timing Analysis and Xilinx Design Constraints

FPGA 3

FPGA-VSTAXDC-ILT (v1.0)

Course Specification

Course Description

This course offers detailed training on the Vivado® software tool flow, Xilinx design constraints (XDC), and static timing analysis (STA). Learn to use good FPGA design practices and all FPGA resources to advantage. Learn to fully and appropriately constrain your design by using industry-standard XDC constraints. Learn how the Vivado IDE design database is structured and learn to traverse the design. Create appropriate timing reports to perform full STA and how to appropriately synthesize your design.

You will also learn the FPGA design best practices and skills to be successful using the Vivado Design Suite. This includes the necessary skills to improve design speed and reliability, including: system reset design, synchronization circuits, optimum HDL coding techniques, and timing closure techniques using the Vivado software. This course encapsulates this information with an UltraFast™ design methodology case study. The UltraFast design methodology checklist is also introduced.

Level – FPGA 3

Course Duration – 3 days

Course Part Number – FPGA-VSTAXDC-ILT

Who Should Attend? – FPGA designers with intermediate knowledge of HDL and FPGA architecture, and some experience with the Xilinx Vivado Design Suite

Prerequisites

- *Essentials of FPGA Design* course or equivalent knowledge of FPGA architecture features; the Vivado software flow; basic FPGA design techniques; basic clock, input, and output timing constraints, and the Constraints Editor
- Intermediate HDL knowledge (VHDL or Verilog)
- Solid digital design background

Optional Videos

- Basic HDL Coding Techniques (parts 1 and 2)*
- Power Estimation*

Software Tools

- Vivado Design or System Edition 2015.3

Hardware

- Architecture: UltraScale™ and 7 series FPGAs**
- Demo board: None**

* Go to www.xilinx.com/training and click the FPGA Design link under Online Training to view these videos.

** This course focuses on the UltraScale and 7 series architectures. Check with your local Authorized Training Provider for specifics or other customizations.

After completing this comprehensive training, you will have the necessary skills to:

- Use good alternative design practices to improve design reliability
- Increase performance by utilizing FPGA design techniques
- Describe the details of Vivado IDE database objects
- Identify Tcl commands for interacting with the database
- Apply complete Xilinx design constraints (XDC), including timing exceptions, false paths, and multi-cycle path constraints
- Utilize static timing analysis (STA) to analyze timing results
- Pinpoint design bottlenecks by using appropriate timing reports
- Apply advanced I/O timing constraints to meet performance goals
- Describe different synthesis options and how they can improve design performance
- Describe the UltraFast design methodology checklist
- Identify key areas to optimize your design to meet your design goals and performance objectives
- Define a properly constrained design
- Optimize HDL code to maximize the FPGA resources that are inferred and meet your performance goals
- Build resets into your system for optimum reliability and design speed
- Build a more reliable design that is less vulnerable to metastability problems and requires less design debugging later in the development cycle
- Use Vivado Design Suite reports and utilities to full advantage, especially the Clock Interaction report
- Identify timing closure techniques using the Vivado Design Suite
- Describe how the Xilinx design methodology techniques work effectively through case study/lab experience

Course Outline

Day 1

- Review of Essentials of FPGA Design
- UltraFast Design Methodology Summary
- FPGA Design Techniques
- Accessing the Design Database
- Demo: Finding Objects
- Demo: Object Properties
- Demo: Object Connectivity
- **Lab 1**: Vivado IDE Database
- Demo: Clock Creation and Basic Static Timing Analysis
- Static Timing Analysis and Clocks
- Demo: Generated Clocks
- **Lab 2**: Vivado IDE Clocks

Day 2

- Inputs and Outputs
- **Lab 3:** I/O Constraints
- Timing Exceptions
- Demo: Timing Exceptions
- **Lab 4:** Timing Exceptions
- Synthesis Techniques

Day 3

- UltraFast Design Methodology Case Study
- Demo: UltraFast Design Methodology Checklist
- HDL Coding Techniques
- Reset Methodology
- **Lab 5:** Resets
- **Lab 6:** SRL and DSP Inference
- Synchronization Circuits and Reports
- Demo: Report CDC Analysis and Clock Interaction Report
- Timing Closure
- Demo: Performance Baselining
- Timing Closure and Design Conversion Lab Introduction
- **Lab 7:** Timing Closure and Design Conversion
- Appendix: Pipelining lab
- Appendix: Synchronization Circuits & the Clock Interaction Report
- Appendix: Replication, Fanout, and Physical Optimization

Lab Descriptions

- **Lab 1**: Vivado IDE Database – Explore the Vivado IDE database using Tcl commands. Use the Tcl Console to evaluate and enter IOB properties.

- **Lab 2**: Vivado IDE Clocks – Create complete XDC constraints for the clocking resources in a design. Implement the design and use the available clocking reports to verify results. Understand the first step in the Xilinx baselining recommendation.
- **Lab 3**: I/O Constraints – Create input and output constraints for a source-synchronous design by using the Timing Constraints utility. You will also generate useful timing reports to verify the timing results. Understand the second step in the baselining recommendation.
- **Lab 4**: Timing Exceptions – Use the Timing Constraints window to enter timing exceptions in the XDC format. You will also generate a useful timing report to verify the timing results. Understand the third and last step in the baselining recommendation.
- **Lab 5:** Resets – Investigate the proper design and use of resets. Examine the impact of seeing a design built originally with asynchronous resets, having resets removed, and finally with synchronous resets only used where necessary.
- **Lab 6:** SRL and DSP Inference – Evaluate the implementation results of a design that uses asynchronous resets and infers more dedicated hardware resources when resets are selectively removed from the design. You will also learn how to infer the DSP hardware resources for other common functions required by most FPGA designs.
- **Lab 7:** Timing Closure and Design Conversion – Learn how a generic processor design was optimized for the 7 series device architecture with basic design changes that impacted the dedicated hardware usage, design speed, and the device utilization.

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