Designing with Xilinx Serial Transceivers

Connectivity 3

CONN-TRX (v1.0)

Course Specification

Course Description

Learn how to employ serial transceivers in UltraScale™ and UltraScale+™ FPGA designs or Zynq® UltraScale+ MPSoC designs.

The focus is on:

- Identifying and using the features of the serial transceiver blocks, such as 8B/10B and 64B/66B encoding, channel bonding, clock correction, and comma detection
- Utilizing the Transceivers Wizards to instantiate transceiver primitives
- Synthesizing and implementing transceiver designs
- Taking into account board design as it relates to the transceivers
- Testing and debugging

Level – Connectivity 3

Course Duration – 2 days

Course Part Number – CONN-TRX

Who Should Attend? – FPGA designers and logic designers

Prerequisites

- Verilog experience (or the *Designing with Verilog* or the *Designing with VHDL* course)
- Familiarity with logic design (state machines and synchronous design)
- Basic knowledge of FPGA architecture and Xilinx implementation tools are helpful
- Familiarity with serial I/O basics and high-speed serial I/O standards is also helpful

Software Tools

- Vivado® System Edition 2020.1
- Mentor Graphics Questa Advanced Simulator 10.7

Hardware

- Architecture: all UltraScale Architectures
- Demo board: Kintex® UltraScale FPGA KCU105 board or Zynq UltraScale+ MPSoC ZCU104 board*

* This course focuses on the UltraScale architectures. Check with your local Authorized Training Provider for the specifics of the in-class lab board or other customizations.

After completing this comprehensive training, you will have the necessary skills to:

- Describe and use the ports and attributes of the serial transceivers in Xilinx FPGAs and MPSoCs
- Effectively use the following features of the gigabit transceivers:
  - 64B/66B and other encoding/decoding, comma detection, clock correction, and channel bonding
  - Pre-emphasis and receive equalization
- Use the Transceivers Wizards to instantiate GT primitives in a design
- Access appropriate reference material for board design issues involving signal integrity and the power supply, reference clocking, and trace design
- Use the IBERT design to verify transceiver links on real hardware

Course Outline

Day 1

- UltraScale, UltraScale+, Zynq UltraScale+ Device Transceivers Overview
- UltraScale, UltraScale+, Zynq UltraScale+ Device Transceivers Clocking and Resets
- Transceiver IP Generation – Transceiver Wizard
- **Lab 1:** Transceiver Core Generation
- Transceiver Simulation
- **Lab 2:** Transceiver Simulation
- PCS Layer General Functionality
- PCS Layer Encoding
- **Lab 3:** 64B/66B Encoding

Day 2

- Transceiver Implementation
- **Lab 4**: Transceiver Implementation
- PMA Layer Details
- PMA Layer Optimization
- **Lab 5**: IBERT Design
- Transceiver Test and Debugging
- **Lab 6**: Transceiver Debugging
- Transceiver Board Design Considerations
- Transceiver Application Examples

- Optional: Additional modules on Virtex® UltraScale+ FPGA GTM transceiver architecture and functionality

Lab Descriptions

- **Lab 1:** Transceiver Core Generation – Use the Transceivers Wizard to create instantiation templates.
- **Lab 2:** Transceiver Simulation – Simulate the transceiver IP by using the IP example design.
- **Lab 3:** 64B/66B Encoding – Generate a 64B/66B transceiver core by using the Transceivers Wizard, simulate the design, and analyze the results.
- **Lab 4:** Transceiver Implementation – Implement the transceiver IP by using the IP example design.
- **Lab 5:** IBERT Design – Verify transceiver links on real hardware.
- **Lab 6:** Transceiver Debugging – Debug transceiver links.

Register Today

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