



Virtex-5 Platform FPGA Family Technical Backgrounder

The age of digital convergence has accelerated the industry's receptivity to and dependence on the fundamental value propositions of FPGAs: flexibility, field upgradeability, parallel processing performance, faster time-to-market, risk mitigation, support of evolving standards, and lower system costs. To accommodate the demand for continued improvements in performance, capacity, power and cost within the growing community of equipment and system vendors riding the digital convergence wave, Xilinx has endeavored to stay a step ahead in every category with leading-edge product introductions in the Virtex™ Series of FPGAs.

Each new evolutionary step within the Virtex family has combined the inherent value of state-of-the-art process technologies with innovative design and a deeper understanding of the applications they serve to deliver solutions that meet our customer's design challenges and requirements.

More than Moore

In the past, moving to the next process node provided a substantial amount of the performance boost. Today, simply moving down the process technology curve in accordance with Moore's Law is not enough. In order to address leading-edge system integration, performance, power and functionality requirements, architectural innovations are also needed to address the design challenges presented by 65-nanometer (nm) technology.

This technology brief reveals the innovative, if not daring steps, Xilinx has taken to evolve a core technology strategy that has served our customers through four previous Virtex generations and 20 years of market-leading FPGA development.

Built upon 65-nm triple-oxide technology, the Company's proven, modular ASMBL™ architecture and revolutionary new ExpressFabric™ technology, Virtex-5 FPGAs offer the ultimate system integration platform to meet the growing need for programmable systems that cut development cycles, enable adoption to changing standards, and extend product lifetimes through field upgradeability. Virtex-5 FPGAs offer unprecedented performance and density gains – at speeds on average 30 percent faster and 65 percent increased capacity over previous generation 90-nm FPGAs. Notably, this breakthrough performance has been achieved while reducing dynamic power consumption by 35 percent and consuming 45 percent less area than previous generation devices.

The Virtex-5 family offers four new domain-optimized platforms that will provide a wide selection of devices with an optimal mix of logic, I/Os and hardened IP blocks for logic-intensive, embedded processing, digital signal processing (DSP), and serial connectivity applications. The following sections discuss in detail the technical innovations behind Virtex-5 LX, the first of the four domain-optimized platforms that Xilinx introduced on May 15, 2006.

Layers of Innovation

To communicate the depth and breadth of innovation required by Virtex-5 LX Platform FPGAs, this brief is organized in five sections:

Section I: Process Technology

- 1.0-V core, 12-layer metal, full low-K dielectric
- Second-generation triple-oxide technology
- Third-generation nickel-silicide self-aligned gate structure
- New mobility-engineered (strained) transistor technology
- Dual-foundry strategy

Section II: Architectural Innovations

- ASMBL Architecture
- New 65-nm ExpressFabric technology

Section III: Hardened IP

- Expanded Dual-Port Block RAM / FIFO
- New 550 MHz Clock Management Tile
- Second-generation SelectIO™ technology
- Second-generation DSP Slice

Section IV: Packaging

- Second-generation Sparse Chevron technology

Section V: Solutions

- Xilinx ISE™ Fmax Technology
- Xilinx PlanAhead™ Design and Analysis Software
- Partner Solutions

These innovations combine to deliver the highest performance, low power, low system cost and maximum productivity to address high density, high performance system-on-chip (SoC) designs that are at the heart of core infrastructure applications that address digital convergence or triple play.

Section I: 65-nm Process Innovations

The move to 65-nm manufacturing involved a composite of technological innovations and changes to deliver the performance and integration levels required by our high-end FPGA customers while keeping leakage currents and power consumption relatively equivalent to the current 90-nm Virtex-4 devices.

Key technological changes contributing to the increased performance and the reduction of leakage current include:

- Low-k inter-metal dielectrics throughout 11 layers of copper interconnect to minimize signal crosstalk²

- Reduction of the core voltage to 1.0-V;
- A new nickel-silicide self-aligned gate structure that lowers the gate resistance and minimizes some of the manufacturing margins that might otherwise detract from the transistor performance;
- The use of strained silicon to deliver faster performance without the need to physically reduce device dimensions, thereby avoiding the excessive leakage currents traditionally seen with ultra-small features; and
- Development of a new generation of triple-oxide technology.

The triple-oxide technology originally developed with the Virtex-4 family addresses the fact that not all transistors on an FPGA need to switch at maximum speed. Thus, ultra-thin gate oxides are used on the highest-performance transistors, while the two thicker oxide layers (and therefore less prone to large amounts of leakage current) are used for I/O and configuration transistors, as well as moderate-performance logic devices in the core of the FPGA.

Dual-Foundry Strategy

One of the innovations involved with 65-nm process development is more a business strategy than a technological innovation, yet the end result will most certainly provide benefits every bit as dramatic as any of the design innovations attributable to the Virtex-5 family. The dual-foundry strategy employed by Xilinx continues to pay dividends with unsurpassed access to leading-edge process technology and manufacturing prowess. Virtex-5 devices will be manufactured at both Xilinx fab partners — Toshiba and UMC. Combined, Toshiba and UMC can support 300-mm/65-nm wafer production in volumes exceeding 15,000 wafers per month. Having two fab sources helps the Company to ensure device supply and guarantees access to the latest process technology.

Section II - Architectural Innovations

ASMBL Architecture

Xilinx created the ASMBL (Advanced Silicon Modular Block) architecture to enable rapid and cost-effective assembly of FPGA platforms with varying feature mixes optimized for different application domains. Through this innovation Xilinx offers a greater selection of devices, enabling customers to select the FPGA with the right mix of features and capabilities for their specific design. This approach significantly increases capability for a given price point, setting a new price-capability standard.

The Virtex-4 family was the first FPGA product line to embody the new ASMBL architecture offering three domain-optimized platforms. The Virtex-4 LX, SX, and FX Platforms were optimized for general logic, signal processing, embedded processing, and high-speed serial connectivity.

The ASMBL architecture breaks through traditional design barriers by:

- Eliminating geometric layout constraints such as dependencies between I/O count and fabric array size;
- Enhancing on-chip power and ground distribution by allowing power and ground to be placed anywhere on the chip; and

- Allowing disparate hard IP blocks to be scaled independent of each other and surrounding resources.

The Virtex-5 family is the second generation to be based on the unique columnar approach provided by the ASMBL architecture and offers four domain-optimized platforms with greater levels of system integration features:

- Virtex-5 LX Platform for high performance logic
- Virtex-5 LXT Platform for high performance logic with serial connectivity
- Virtex-5 SXT Platform for high performance DSP with serial connectivity
- Virtex-5 FXT Platform for embedded processing with serial connectivity

The Virtex-5 LX Platform is available today with each of the remaining platforms slated for the second half of 2006 through the first half of 2007.

New 65-nm Ultra-Fast ExpressFabric Technology

The Virtex-5 FPGA family is based on an all-new 65-nm ExpressFabric technology which offers unprecedented performance and density gains: 65 percent increased logic capacity and speeds over 30 percent faster than the previous generation. Incorporating a look-up table (LUT) with six independent inputs and a new diagonal interconnect structure, the ExpressFabric enables implementation of combinatorial logic in fewer logic levels and connections to neighboring building blocks with fewer hops, as compared to the Virtex-4 architecture. This reduces data path delays and increases the clock speed of designs. Designs are packed more efficiently, thus improving utilization and performance while reducing power consumption. Specifically built to enable wide bus structures found with increasing logic density and integration, the real 6-input LUTs can implement logic, while also implementing larger distributed memories and shift registers.

Xilinx benchmarking and architectural modeling have shown a capacity advantage of 65 percent and performance improvements of 30 percent over Virtex-4 devices. The figure below illustrates a Virtex-5 slice along with the new 6-input LUT structure.

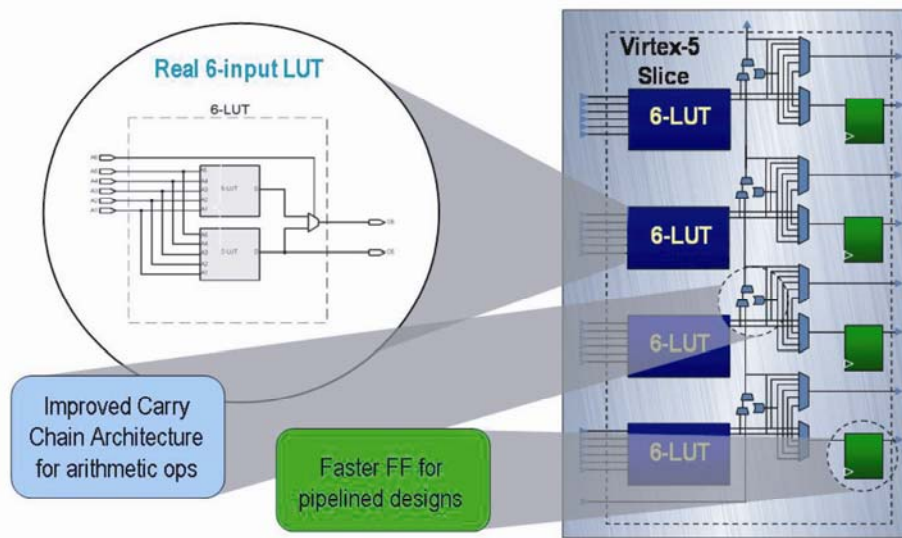


Figure 1: Virtex-5 Slice with new 6-LUT ExpressFabric

Distributed Memory

Virtex-5 CLBs also support distributed memory, or LUTRAM. Each look-up table can be configured to operate as a 64-bit memory, a substantial increase over the 16-bit LUTRAM in Virtex-4 devices. LUTRAM enables very effective, small localized memory for applications that require many small buffers. Because of the structure of the Virtex-5 LUT, each LUT can be configured as a 64x1 or 32x2 RAM.

SRL (Shift Register)

The look-up tables in the Virtex-5 CLB also support SRL32 (or optionally SRL16 x 2) capability in a memory slice (vs. SRL16 in Virtex-4 FPGAs). All four SRLs in a memory slice can be chained together to create a 128-bit shift register. Each SRL is also variable tap.

Interconnect

A new diagonally symmetric interconnect pattern also enhances performance by reaching more places in fewer hops. A comparison of the Virtex-5 FPGA interconnect pattern to the Virtex-4 FPGA pattern (with each box representing a CLB) is shown here:

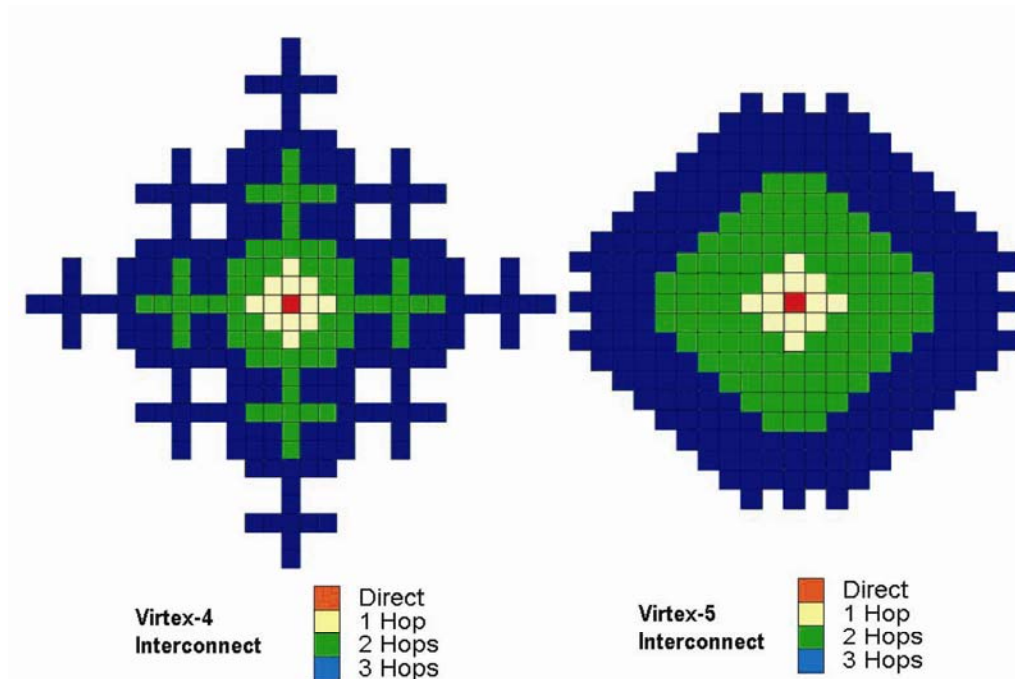


Figure 2: Virtex-5 vs. Virtex-4 Interconnect Architecture

As reflected in the above figure, the more comprehensive routing pattern will allow for more logic connections to be made within two and three hops, thus adding to overall design performance. In addition, the more regular routing pattern makes it easier for the Xilinx ISE™ software to locate the most optimal routes. All interconnect features are transparent to Virtex-5 FPGA customers, but will translate to higher overall performance and easier design routability. Essentially, the Virtex-5 device pattern provides fast, predictable routing based on distance.

Section III: Hardened IP Innovations

Virtex-5 LX is built with an array of embedded hard IP that includes an ultra-fast clocking technology, block RAM and DSP slice, all tuned to 550 MHz.

New High-Density Block RAM/FIFOs

The Block RAM (BRAM) base size in Virtex-5 devices has increased to 36-Kbits, versus 18-Kbits in the previous generation 90-nm Virtex-4 FPGAs. This makes it easier to build larger memory arrays in Virtex-5 devices (i.e., less routing will be required to cascade BRAMs to build internal memory sizes larger than 18-Kbits total). In addition, for most BRAM modes, the 36-Kbit BRAM can be used as two independent 18-Kbit BRAMs, so there is essentially no penalty for designers who wish to build many 18-Kbit or smaller RAM arrays on-chip. Also, the Virtex-5 BRAM can be operated in Simple Dual Port mode (1 Read port and 1 Write port) to effectively double the BRAM bandwidth. The block RAM also has integrated FIFO logic without consuming additional logic resources. Other features include new 64-bit ECC (error checking and correction) and the ability to save power by turning off the 18-Kbit blocks that are unused.

New High-Performance, Low-Jitter Clocking

In the Virtex-5 family, clock management is handled a bit differently than previous generation devices. The Virtex-5 clocking is generated from CMT (Clock Management Tile) blocks. Each CMT contains two DCMs (digital clock managers) and one PLL (phase locked loop) that can drive the global clock buffers or can be cascaded for jitter filtering. The benefits of the CMT are that Virtex-5 clocking will get the best of both worlds: DCM technology for precision delay control and more immunity to noise, and PLL technology for lower jitter clock generation and jitter filtering.

Virtex-5 devices provide up to six CMTs per device, allowing for very flexible clock generation capability. Each CMT is capable of generating clocks up to 550 MHz to support the performance of the Virtex-5 block functions and logic.

Enhanced SelectIO

The Virtex-5 SelectIOs contain many of the popular features found in Virtex-4 devices including Xilinx ChipSync™ Technology, DCI (digitally controlled impedance), Single-Ended, and Differential Support. The target performance for Virtex-5 I/Os is 700Mbps Single Ended (which can be increased to 800 Mbps with a relaxed Duty Cycle Distortion requirement) and 1.25 Gbps differential. Select IO combined with pre-verified IP cores makes it easy to support all popular interface standards and offers flexibility to interface to virtually any external component. For instance, designers can design for PCI, RapidIO, XSBI, SPI4.2 and configure I/Os from 1.5-V to 3.3-V with support for HSTL, LVDS and more. SelectIO also has the flexibility to support multiple electrical standards in the same device with 35 individually configurable I/O banks.

Other SelectIO enhancements include:

- 40 I/O per bank - This is a reduction from the 64 I/O per bank in Virtex-4 devices, thereby providing finer granularity (i.e., allows for more independent standards per device and offers greater flexibility in I/O placement).
- Up to 1,200 packaged SelectIO - Virtex-4 devices reached a maximum SelectIO count of 960. For higher parallel I/O applications the increase in I/O provides additional capability.

Second Generation ChipSync Calibration Circuitry

Virtex-5 SelectIO includes second generation ChipSync technology for reliable synchronization of data and clock as well as adaptive calibration to compensate for changing operating conditions. In Virtex-4 ChipSync logic, programmable IDELAY elements were provided on all inputs in order to facilitate clock-data alignment. In Virtex-5 FPGAs, the block can be programmed to provide input or output delay. Output delay is useful for fixing PCB skew problems or reducing total SSO (simultaneously switched output) noise.

Enhanced DSP Slice

The Virtex-5 DSP48E is based on 25x18 bit multipliers (versus 18x18 in Virtex-4 FPGAs). DSP Slices are cascaded to provide greater multiplier width. The increase to 25x18 can lead to fewer cascade stages, giving higher overall performance and utilization. One example application that can use the wider multiplication capability is floating point, which typically uses 24x24 multipliers. A 24x24 multiplier can be built in Virtex-5 devices using two DSP48E Slices (half the number of required Virtex-4 DSP48 Slices). Single precision floating point support for unsigned 24x24 is actually a subset of 35x35 capability (available with two DSP48E Slices).

Section IV: Packaging Innovations

Sparse Chevron Pinout Architecture

The pinout architecture of the package is responsible for roughly 80 percent of the total noise. The pin distribution incorporated in the Sparse Chevron architecture is a tiled pattern with a regular array of signal, ground and power pins. Figure 3 shows the package pin distribution with the Sparse Chevron architecture introduced with Virtex-4 FPGAs. The signal-to-ground-to-power ratio of the package is 8:1:1. Since both power and ground are equally effective as return signal current paths, the package effectively has a signal-to-return ratio of 4:1. Also, the pins are distributed such that every signal pin is adjacent to a return pin. The close proximity of the return pins to the signal pins ensures that the return current loop is kept to a minimum.

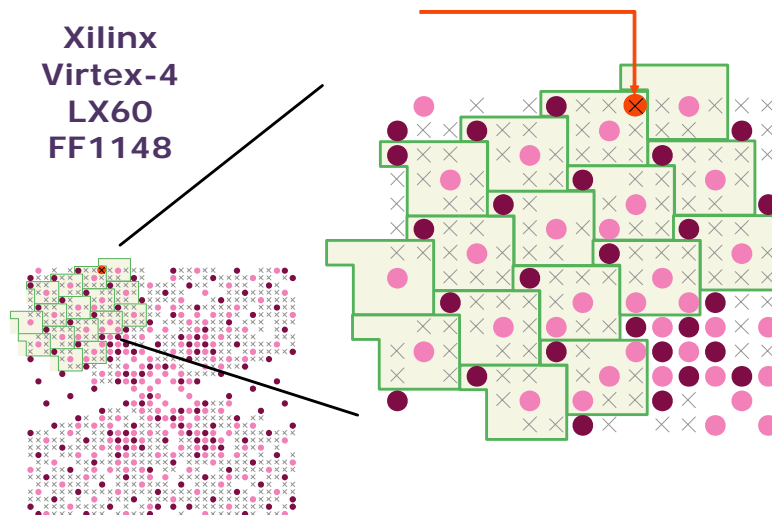


Figure 3: Sparse Chevron Pinout Architecture

Also, the abundance of return paths in any given area of the package provides a low impedance path for the return currents. The Sparse Chevron pinout also confines the noise from an aggressor to a smaller area so the influence of the aggressor drops rapidly with distance. Since crosstalk noise is cumulative, this results in lower total SSN noise.

The Virtex-5 family incorporates a second-generation Sparse Chevron packaging technology that delivers unmatched signal integrity, enhances board routability, improves thermal conductivity, optimized package pinout, and reduces cost with fewer required PCB layers. Sparse Chevron in Virtex-5 devices helps keep system noise under control with a low-noise chip. Its unique power/ground pin pattern minimizes crosstalk and simplifies board layout, while minimizing the risk of costly board redesigns.

Section V: Solutions

Xilinx also provides a complete portfolio of design solutions, including software, IP, development kits and reference designs to reduce the time-to-design closure.

ISE Fmax Technology

ISE Fmax Technology is an industry-unique combination of software and capabilities that delivers:

- 30 percent faster performance than Virtex-4 FPGAs;
- Largest timing margins with ExpressFabric technology and hardened IP blocks;
- Next-generation physical synthesis technology; and
- Faster design closure and better out-of-the-box performance.

ISE Fmax technology introduced in the ISE 8.1i release features innovations that are also applicable to Virtex-5 FPGAs.

- Next-generation physical synthesis optimizations:
 - Design retiming - dynamically moves registers to balance combinatorial logic delays
 - Timing-driven mapping - delivers a more timing-aware placement phase, allowing packing decisions to be made earlier and then revisited when initial results are less than optimal
 - Global optimization - takes a fully-mapped design and improves performance by re-optimizing combinatorial and register logic
 - Logic optimization - uses a combination of logic duplication, logic recombination, element switching, and pin swapping to optimize design performance
- Performance Evaluation Mode - ISE 8.1i out-of-the box delivers on average 37 percent faster design performance for designs with no timing constraints applied
- Xplorer script - Automatically helps find the ideal design results through multiple implementation runs using different place and route settings and constraints
- PlanAhead Design and Analysis Software - an optional design and analysis tool from Xilinx

This industry-unique technology helps solve the number one problem for logic engineers — timing closure, while reducing design time and getting to market faster. The result is the lowest cost in logic design.

Partner Solutions

Based on the vast partner ecosystem developed through nearly a decade of Virtex Series innovation, Xilinx has collaborated closely with partners to produce design tools and evaluation

boards specifically designed to optimize the new features of the Virtex-5 architecture. See related partner Virtex-5 related news from [Synplicity](#), [Mentor Graphics](#) and [Magma Design Automation](#).

Summary

The Virtex-5 platform FPGA family addresses the major technology gaps required to capitalize on the triple play or digital convergence market opportunity. Virtex-5 FPGAs meet the technology requirements for the core infrastructure market and the performance, power and integration needs of high-performance system designs. Designers can choose a FPGA platform with the optimal mix of capabilities for their specific design along with the flexibility, low-cost and time-to-market benefits they have come to expect from FPGAs.

The introduction of Virtex-5 LX Platform is the first step towards addressing this broader market trend. Building on innovations in process technology, architecture and product development methodology, Virtex-5 LX FPGAs deliver unprecedented performance and density gains— at speeds on average 30 percent faster and 65 percent increased capacity over previous generation 90-nm FPGAs – while reducing dynamic power consumption by 35 percent and consuming 45 percent less area.

Virtex-5 Family Device & Software Availability

Delivery of new Virtex-5 Family FPGAs has commenced and will continue through the first half of 2007:

- Virtex-5 LX for high performance logic – *Shipping Now*
- Virtex-5 LXT for high performance logic with serial connectivity – *2nd half of 2006*
- Virtex-5 SXT for high performance DSP with serial connectivity – *2nd half of 2006*
- Virtex-5 FXT for embedded processing with serial connectivity – *1st half of 2007*

Early access software for Virtex-5 LX is available now with general availability in June 2006. Virtex-5 LX FPGA engineering samples are shipping now in the LX50, LX85, and LX110 densities. The Xilinx EasyPath™ program, which offers an additional risk-free cost reduction for high volume production, will be available to customers for each Virtex-5 platform upon volume production. For more information on pricing and availability, please refer to the [Xilinx Virtex-5 LX Platform news release](#) or visit www.xilinx.com/virtex5.