

## MicroBlaze Soft Processor v8.10a *Frequently Asked Questions*

### What is a soft processor?

A soft processor is an Intellectual Property (IP) core that is implemented using the logic primitives of the FPGA. Being soft allows it to have a high degree of flexibility and configurability.

### What is the MicroBlaze soft processor?

The MicroBlaze soft processor is a soft 32-bit RISC processor that is part of the Embedded Development Kit (EDK). EDK also includes other supporting IP as well as tools and GUIs for building FPGA-based embedded systems. EDK is part of the ISE® Design Suite, Embedded Edition software package available from Xilinx.

### What are the key benefits of having a soft FPGA-based processing system?

Being FPGA-based provides many key benefits.

Feature	Benefit
Configurable	Optimize your embedded system: include only the features you need.
Programmable	Like any microprocessor-based system, a function change is as easy as recompiling your C-code.
FPGA-Based	A 32-bit RISC microprocessor plus the rest of your design on a single chip.

Key benefits of using an FPGA-based soft processor

### What's new with the MicroBlaze v8.10a, which is included in the ISE Design Suite: Embedded Edition 13.1?

The new features added to MicroBlaze in this release include ECC (Error Correction Code) and Parity protection. In MicroBlaze designs, the areas that need protection are those that involve Block RAM (BRAM). These features consist of ECC on LMB BRAMs and parity on BRAMs internal to MicroBlaze. LMB memory requires error correction of a single bit since there is no backup of the memory available. The LMB BRAM interface controllers have also been modified to support ECC. This requires external BRAM to support new configurations to include the ECC bits. External BRAM now requires a 40-bit arrangement. For more information, please see the MicroBlaze data sheet.

### How do I purchase the MicroBlaze soft processor core?

MicroBlaze is included with EDK, which is part of the ISE Design Suite: Embedded Edition and System Edition. To learn more about purchasing the ISE Design Suite: Embedded Edition and System Edition visit [www.xilinx.com/ise-embedded](http://www.xilinx.com/ise-embedded). Additionally, existing ISE Design Suite customers can purchase a stand-alone version of the EDK.

### How is MicroBlaze licensed?

The MicroBlaze soft processor is included as part of the Xilinx ISE Design Suite: Embedded Edition and System Edition and is shipped under the Xilinx Core Site License agreement. This license allows you to use MicroBlaze in an unlimited number of Xilinx FPGA designs at the licensed site without any additional royalties.

### Is source code available?

No.

### What is MicroBlaze performance? How many Dhrystone MIPS can it achieve?

MicroBlaze performance depends on the configuration of the processor and the target FPGA architecture and speed grade. All of these factors affect the Fmax (ultimate clock speed) achievable by the embedded processor design. Dhrystone MIPS (DMIPS) are directly related to the Fmax of the design and DMIPS/MHz is number that is often associated with embedded processors.

In the case of MicroBlaze, we have a performance-optimized version with a 5-stage pipeline and an area-optimized version with a 3-stage pipeline. The DMIPs / MHz for each version are shown:

Performance Optimized with Branch Optimizations	1.30 DMIPS/MHz
Performance Optimized	1.19 DMIPS/MHz
Area Optimized	0.95 DMIPS/MHz

### How many MicroBlaze processors can run on a single FPGA device?

The number of MicroBlaze processors on a single FPGA is only limited by the size of the FPGA. The MicroBlaze Debug Module (MDM) allows debugging of up to eight MicroBlazes at a time.

### Can I create my own peripheral or coprocessor?

Yes. The MicroBlaze soft processor includes several optional interfaces that allow you to connect your own custom peripherals and coprocessors, as well as Xilinx provided peripherals.

Xilinx Platform Studio, part of EDK, includes the "Create IP Wizard" which greatly simplifies the creation of such peripherals and coprocessors. The Create IP Wizard will support AXI interfaces beginning with ISE Design Suite 13.1. Until then, there is a solution record available for guidance on creating AXI IP. Consult <http://www.xilinx.com/support/answers/37425.htm> for more information

### What kinds of peripherals are available for use with MicroBlaze?

The Platform Studio comes with a standard set of peripherals including timers, UARTs, interrupt controllers, GPIOs, and external flash and memory controllers. Some of the more complex cores have additional one-time licensing associated. Evaluation licenses are available for these peripherals.

### What types of memory does MicroBlaze support?

The MicroBlaze standard memory controller peripheral set includes SDR, DDR, DDR2, DDR3, SRAM and Flash controllers. In addition, MicroBlaze makes use of the on-chip block RAMs.

### What is the easiest way to connect to an external chip with a non-standard interface?

Platform Studio includes a piece of IP called the External Peripheral Controller. The External Peripheral Controller is a configurable piece of IP designed to allow easy hook-up to external peripherals with non-standard interfaces.

### What sort of compilers and debugging tools are available for MicroBlaze?

To build your designs, EDK includes the full GNU suite including a C/C++ compiler, debugger, and assembler as well as all of the standard libraries. For debugging, EDK also includes the Eclipse-based Software Development Kit (SDK) as well as Chipscope Pro™, the on-chip FPGA bus and logic analyzer.

### What operating systems have been ported to MicroBlaze?

PetaLogix PetaLinux (Linux 2.6.x), Micrium uC/OS-II and Express Logic ThreadX are some of the operating systems that support MicroBlaze. Please refer to

<http://www.xilinx.com/ise/embedded/epartners/listing.htm#RTOS> for a complete, up-to-date listing.

### **Can I build multiprocessor systems?**

Yes, multiprocessor systems can be created manually or by using Base System Builder (one of the wizards included in Platform Studio). Base System Builder will build a custom PLB-based dual-processor system with just a few mouse clicks. Note that Base System Builder will not support the creation of dual processor AXI systems until 13.2. Dual processor AXI systems can still be built manually by building a single processor AXI system in Base System Builder, then adding the second processor manually.

### **Can multiprocessor MicroBlaze systems communicate easily?**

Yes. Platform Studio includes Mailbox, MUTEX, dual-port Block RAM and Multi-Port Memory Controller IP for all levels of interprocessor communication. Base System Builder will allow you to include these peripherals in a dual-processor AXI embedded system.

Another way in which multi-MicroBlaze systems can communicate is by using the direct point-to-point Fast Simplex Links (FSLs) for inter-processor communication. MicroBlaze contains a Processor Version Register which includes fields for: Processor ID, configuration/user/processor info (e.g. cache size etc), version number and other internal information that can be used to identify a particular MicroBlaze core in a multi-core system.

### **Does MicroBlaze Have a Floating Point Unit?**

An optional IEEE-754 compatible single precision Floating Point Unit (FPU) is available for MicroBlaze. The tightly integrated FPU combines high performance and low latency. The MicroBlaze FPU is a configurable part of the MicroBlaze processor core and is included with Platform Studio at no extra cost. The MicroBlaze FPU can be added in Base System Builder with a single mouse click.

### **Why would I want to use the MicroBlaze FPU?**

Many applications in the embedded arena are floating point intensive. For such applications, executing floating point operations in software is slow. Using the MicroBlaze with the FPU for such applications provides a huge boost in performance (in some cases up to 40x speedup over software floating-point).

### **Is the MicroBlaze FPU IEEE-754 compliant?**

The MicroBlaze FPU is IEEE-754 compatible, but not fully compliant. It deviates from the standard in certain infrequent corner cases:

- An operation on a quiet NaN will return a fixed NaN, not one of the operands.
- Only round-to-nearest mode is supported.
- Denormalized operands are not supported. If exceptions are enabled, a denormal exception will be generated. Otherwise a quiet NaN will be returned.
- Denormalized results are flushed to zero.
- If necessary these corner cases can be handled using software libraries called from exception handlers.

### **Is the MicroBlaze FPU configurable?**

Yes. IEEE-754 compatibility is the baseline FPU configuration. This functionality can be augmented with support for FLT, FINT and FSQRT instructions.

### **Do I need any special floating point libraries to use the FPU?**

No. The floating point operations are part of the MicroBlaze ISA and are automatically recognized by the compiler. Any operation on the C data type 'float' will be automatically inferred by the compiler to use the FPU.

### **How Would I Support Custom Instructions in MicroBlaze?**

User-defined instructions are fairly complex solutions to hardware acceleration. The MicroBlaze soft processor uses a more robust and versatile co-processor solution based on the optional Fast Simplex Link (FSL) to achieve the same objective.

The low latency FSL's can connect up to sixteen co-processors, each of which can naturally perform more than one custom function. A co-processor function can also go beyond the "two operands and a result" structure of user-defined instructions. Finally, there is less risk of harming the processor maximum frequency with a co-processor since it is not part of the pipeline.

#### **What are the different Caching options in MicroBlaze?**

MicroBlaze has optional Instruction and Data caches. The Data Cache supports both write through (smaller footprint) and write-back (higher performance) operation. In v7.30, logic has been added to further boost the performance of the caches. Instruction Stream Buffers will speculatively fetch Instruction Cache lines in advance of the processor actually needing them. Victim Caches store recently flushed cache lines locally. If they are needed again, they are available locally since an access to external memory is not needed.

#### **How Are Branches Optimized in the MicroBlaze Architecture?**

*Branch prediction is employed on architecture with long pipelines in which branches are resolved late in the pipeline.* In the MicroBlaze core, however, branches are resolved in the third stage. As a result, a taken branch can have at most a two cycle penalty. This two cycle penalty is further reduced by the automatic use of branches with delay slot instructions by the compiler. As a result, the MicroBlaze core has a zero cycle penalty on not taken branches, and a one cycle penalty on taken branches with a delay slot instruction.

MicroBlaze also includes an optional Branch Target Cache which stores up to 2048 (the actual number is user-programmable) previously executed branches. Depending on your application, this can provide a substantial boost in code execution performance.

#### **Why a Performance-optimized (5-stage) or an Area-optimized (3-stage) MicroBlaze core?**

MicroBlaze v8.10a is the latest version of the MicroBlaze soft processor. This core is configurable for performance-optimized (5-stage pipeline) or cost-focused (3-stage pipeline) applications. It is 100% binary backward compatible with previous MicroBlaze core releases. The additional pipeline stages in the performance-optimized mode help lower the clock per instruction (CPI) which improves the overall processor performance to 1.19 DMIPS/MHz or 1.30 DMIPS/MHz with new branch optimizations. MicroBlaze is at its smallest core size when used with 3 pipeline stages. This is an ideal choice for cost-focused MicroBlaze applications.

#### **Where can I get additional information on MicroBlaze?**

Visit [www.xilinx.com/microblaze](http://www.xilinx.com/microblaze) for more information.