

MicroBlaze Soft Processor v7.20 *Frequently Asked Questions*

What is a soft processor?

A soft processor is an Intellectual Property (IP) core that is implemented using the logic primitives of the FPGA. Being soft allows it to have a high degree of flexibility and configurability.

What is the MicroBlaze soft processor?

The MicroBlaze soft processor is a soft 32-bit RISC processor that is part of the Embedded Development Kit (EDK). EDK also includes other supporting IP as well as tools and GUIs for building FPGA-based embedded systems. EDK is part of the ISE Design Suite, Embedded Edition software package available from Xilinx.

What are the key benefits of having a soft FPGA-based processing system?

Being FPGA-based provides many key benefits.

Feature	Benefit
Configurability	Trade off size versus performance
Programmability	Get to market faster, stay in market longer
FPGA-Based	Construct an embedded system and easily integrate with your own logic

Key benefits of using an FPGA-based soft processor

What's new with the MicroBlaze 7.20, which is included in the ISE Design Suite: Embedded Edition 11?

New features for MicroBlaze version 7.20 are as follows:

- MicroBlaze / Multi-Port Memory Controller cross-optimization, including write-back cache. This combination of features provides a smaller footprint, higher performance solution.
- Base System Builder now builds dual-processor systems.
- Debug enhancements for more efficient trace port output
- Atomic Test and Set Memory Instructions, which are used for spin-locking and functions that require mutual exclusion.

How do I purchase the MicroBlaze soft processor core?

MicroBlaze is included with EDK, which is part of the ISE Design Suite: Embedded Edition. To learn more about purchasing the ISE Design Suite: Embedded Edition visit www.xilinx.com/ise-embedded. Additionally, existing ISE Design Suite customers can purchase a stand-alone version of the EDK.

How is MicroBlaze licensed?

The MicroBlaze soft processor is included as part of the Xilinx ISE Design Suite: Embedded Edition and is shipped under the Xilinx Core Site License agreement. This license allows you to use MicroBlaze in an unlimited number of Xilinx FPGA designs at the licensed site without any additional royalties.

Is source code available?

No. The MicroBlaze soft processor is a highly optimized design, specifically targeted to Xilinx FPGAs. There is a high degree of integration within the various EDK tools. User modifications to the MicroBlaze soft processor have the potential to break that integration.

What is MicroBlaze performance? How many Dhrystone MIPS can it achieve?

MicroBlaze performance depends on the configuration of the processor and the target FPGA architecture and speed grade. All of these things affect the Fmax (ultimate clock speed) achievable by the embedded processor design. Dhrystone MIPS (DMIPS) are directly related to the Fmax of the design and DMIPS/MHz is number that is often associated with embedded processors.

In the case of MicroBlaze, we have a 3-stage pipeline version and a 5-stage pipeline version, and their DMIPS/MHz numbers are:

3-stage pipeline	0.95 DMIPS/MHz
5-stage pipeline	1.19 DMIPS/MHz

How many logic resources does MicroBlaze use?

This will depend on the configured options and target FPGA. Please refer to http://www.xilinx.com/products/design_resources/proc_central/microblaze_per.htm.

How many MicroBlaze processors can run on a single FPGA device?

The number of MicroBlaze processors on a single FPGA is only limited by the size of the FPGA. The MicroBlaze Debug Module (MDM) allows debugging of up to eight MicroBlazes at a time.

Can I create my own peripheral or coprocessor?

Yes. The MicroBlaze soft processor includes several optional interfaces that allow you to connect your own custom peripherals and coprocessors, as well as Xilinx provided peripherals.

Xilinx Platform Studio, part of EDK, includes the "Create IP Wizard" that greatly simplifies the creation of such peripherals and coprocessors.

What kinds of peripherals are available for use with MicroBlaze?

The Platform Studio comes with a standard set of peripherals including timers, UARTs, interrupt controllers, GPIOs, and external flash and memory controllers. A few complex cores have additional one time licensing associated, but are available for time limited evaluation at no extra cost.

What types of memory does MicroBlaze support?

The MicroBlaze standard memory controller peripheral set includes SDR, DDR, DDR2, SRAM and Flash controllers.

What is the easiest way to connect to an external chip with a non-standard interface?

Platform Studio includes a piece of IP called the External Peripheral Controller. The External Peripheral Controller is a configurable piece of IP designed to allow easy hook-up to external peripherals with non-standard interfaces.

What sort of compilers and debugging tools are available for MicroBlaze?

To build your designs, EDK includes the full GNU suite including a C/C++ compiler, debugger, and assembler as well as all of the standard libraries (depending on the supported I/O devices). For debugging, EDK also includes the Eclipse-based Software Development Kit (SDK) as well as Chipscope Pro™, the on-chip FPGA bus and logic analyzer.

What operating systems have been ported to MicroBlaze?

LynuxWorks Blue Cat Linux2.6, Mentor Nucleus, Express Logic ThreadX, Micrium uC/OS-II, PataLogix uClinux and PetaLinux are some of the operating systems that support MicroBlaze. Please refer to <http://www.xilinx.com/ise/embedded/epartners/listing.htm#RTOS> for a complete, up-to-date listing.

Can I build multiprocessor systems?

Yes, and beginning with 11.1, Base System Builder (one of the wizards included in Platform Studio) will build a custom dual-processor system with just a few mouse clicks. Previous versions of Platform Studio allowed the construction of multiprocessor systems also. Base System Builder in 11.1 makes it much easier.

Can multiprocessor MicroBlaze systems communicate easily?

Yes. Platform Studio includes Mailbox, MUTEX, dual-port Block RAM and Multi-Port Memory Controller IP for all levels of interprocessor communication. Base System Builder will allow you to include these peripherals in a dual-processor embedded system.

Another way in which multi-MicroBlaze systems can communicate is by using the direct point to point Fast Simplex Links (FSLs) for inter-processor communication. In the MicroBlaze v7.20 core, the Processor Version Register contains: Processor ID, configuration/user/processor info (e.g. cache size etc), version number and other internal information that can be used to identify a particular MicroBlaze core in a multi-core system.

Does MicroBlaze Have a Floating Point Unit?

An optional IEEE-754 compatible single precision Floating Point Unit (FPU) is available for MicroBlaze. The tightly integrated FPU combines high performance and low latency. The MicroBlaze FPU is a configurable part of the MicroBlaze v7.20 processor core and is included with Platform Studio at no extra cost. The MicroBlaze FPU can be added in Base System Builder with a single mouse click.

Why would I want to use the MicroBlaze FPU?

Many applications in the embedded arena are floating point intensive. For such applications, executing floating point operations in software is expensive. Using the MicroBlaze for such applications provides a huge boost in performance (in some cases up to 40x speedup over software floating-point).

Is the MicroBlaze FPU IEEE-754 compliant?

The MicroBlaze FPU is IEEE-754 compatible, but not fully compliant. It deviates from the standard in certain infrequent corner cases:

- An operation on a quiet NaN will return a fixed NaN, not one of the operands.
- Only round-to-nearest mode is supported.
- Denormalized operands are not supported. If exceptions are enabled, a denormal exception will be generated. Otherwise a quiet NaN will be returned.
- Denormalized results are flushed to zero.
- If necessary these corner cases can be handled using software libraries called from exception handlers.

Is the MicroBlaze FPU configurable?

Yes. IEEE-754 compatibility is the baseline FPU configuration. This functionality can be augmented with support for FLT, FINT and FSQRT instructions.

Do I need any special floating point libraries to use the FPU?

No. The floating point operations are part of the MicroBlaze ISA and are automatically recognized by the compiler. Any operation on the C data type 'float' will be automatically inferred by the compiler to use the FPU.

How Would I Support Custom Instructions in MicroBlaze?

User-defined instructions are fairly complex solutions to hardware acceleration. The MicroBlaze soft processor uses a more robust and versatile co-processor solution based on the optional Fast Simplex Link (FSL) to achieve the same objective.

The low latency FSL's can connect up to sixteen co-processors, each of which can naturally perform more than one custom function. A co-processor function can also go beyond the "two operands and a result" structure of user-defined instructions. Finally, there is less risk of harming the processor maximum frequency with a co-processor since it is not part of the pipeline.

How Are Branches Optimized in the MicroBlaze Architecture

Branch prediction is employed on architecture with long pipelines in which branches are resolved late in the pipeline. In the MicroBlaze core, however, branches are resolved in the third stage. As a result, a taken branch can have at most a two cycle penalty. This two cycle penalty is further reduced by the automatic use of branches with delay slot instructions by the compiler. As a result, the MicroBlaze core has a zero cycle penalty on not taken branches, and a one cycle penalty on taken branches with a delay slot instruction.

Why a Performance-optimize (5-stage) or Size-optimized (3-stage) MicroBlaze core?

MicroBlaze v7.20 is the latest version of the MicroBlaze soft processor. This core is configurable for performance-optimized (5-stage pipeline) or cost-focused (3-stage pipeline) applications. It is 100% binary backward compatible with previous MicroBlaze core releases. The additional pipeline stages in the performance-optimized mode help lower the clock per instruction (CPI) which improves the overall processor performance to 1.19 DMIPS/MHz. The MicroBlaze v7.20 is at its smallest core size when used with 3 pipeline stages. This is an ideal choice for cost-focused MicroBlaze Spartan applications.

Where can I get additional information on MicroBlaze?

Visit www.xilinx.com/microblaze for more information.