



## **MicroBlaze Soft Processor v7**

### ***Frequently Asked Questions***

#### **What is a soft processor?**

A soft processor is an Intellectual Property (IP) core that is implemented using the logic primitives of the FPGA. Key benefits of using a soft processor include configurability to trade between price and performance, faster time to market, easy integration with the FPGA fabric, and avoiding obsolescence.

#### **How do I purchase the MicroBlaze soft processor core?**

MicroBlaze parameterized netlist is licensed as part of the Xilinx Embedded Development Kit. This product has the full configurability and functionality of MicroBlaze and is provided with source file encryption. To purchase the EDK, visit [www.xilinx.com/edk](http://www.xilinx.com/edk).

Non-encrypted VHDL source files for Xilinx FPGAs can be purchased separately.

#### **What is the license for MicroBlaze?**

The MicroBlaze soft processor, is included as part of the Xilinx Embedded Development Kit (EDK) and is shipped under the Xilinx Core Site License agreement. This license allows you to use MicroBlaze in an unlimited number of Xilinx FPGA designs at the licensed site without any additional royalties.

#### **What is the MicroBlaze performance? How many Dhrystone MIPS can it achieve?**

MicroBlaze performance depends on the configuration of the processor and the target FPGA architecture and speed grade. Please refer to the latest MicroBlaze performance table in the MicroBlaze 'sell sheet' collateral.

#### **How many logic resources does MicroBlaze use?**

This will depend on the configured options and target FPGA. Please refer to [http://www.xilinx.com/ipcenter/processor\\_central/microblaze/performance.htm](http://www.xilinx.com/ipcenter/processor_central/microblaze/performance.htm).

#### **How many MicroBlaze processors can run on a single FPGA device?**

The number of MicroBlaze processors on a single FPGA is only limited by the size of the FPGA. The MicroBlaze Debug Module (MDM) allows debugging of eight MicroBlazes at a time.

#### **Can I create my own peripheral or coprocessor?**

Yes. The MicroBlaze soft processor includes several configurable interfaces that allow you to connect your own custom peripherals and coprocessors, as well as Xilinx provided peripherals.

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Xilinx Platform Studio, part of the EDK, includes wizards that simplify the creation of such peripherals and coprocessors.

### **What kinds of peripherals are available for use with MicroBlaze?**

The Embedded Development Kit comes with a standard set of peripherals including timers, UARTs, interrupt controllers, GPIOs, and external flash and memory controllers. A few complex cores have additional one time licensing associated, but are available for time limited evaluation at no extra cost. The Xilinx Platform Studio development tool, included in the EDK, provides wizards to create and integrate your own peripherals.

### **What types of memory does MicroBlaze support?**

The MicroBlaze standard peripheral set includes SDR, DDR, DDR2, SRAM and Flash controllers.

### **What sort of compilers and debugging tools are available for MicroBlaze?**

The Embedded Development Kit (EDK) includes the full GNU suite including a C compiler, debugger, and assembler as well as all of the standard libraries (depending on the supported I/O devices). EDK includes a software development kit with an Eclipse based IDE. For debugging, the Xilinx Chipscope Pro™ on-chip FPGA logic analyzer can be purchased separately.

### **What operating systems have been ported to MicroBlaze?**

The Mentor Nucleus, ThreadX, Micrium uC/OS-II, embedded Linux2.6, uClinux and ultron are some of the real time operating system to support the Xilinx MicroBlaze soft processor core. Please refer to <http://www.xilinx.com/ise/embedded/epartners/listing.htm#RTOS>.

### **Can multiple MicroBlaze processors communicate easily?**

Yes. One way is to use messaging through shared memory, another is to use the direct point to point Fast Simplex Links (FSLs) for inter-processor communication. In MicroBlaze v7.00 core, the Processor Version Register contains: Processor ID, configuration/user/processor info (e.g. cache size etc), version number and other internal information that can be used to identify a particular MicroBlaze core in a multi-core system.

### **What is the MicroBlaze FPU?**

The MicroBlaze soft processor provides an optional IEEE-754 compatible single-precision Floating-Point Unit (FPU). The tightly integrated design combines performance, low latency, and low cost. The MicroBlaze FPU is a configurable part of the MicroBlaze v7.00 processor core and is included at no extra cost.

### **Why would I want to use the MicroBlaze FPU?**

Many applications in the embedded arena are floating point intensive. For such applications, executing floating point operations in software is expensive. Using the MicroBlaze for such applications provides a huge boost in performance (in some cases up to 40x speedup over software floating-point).

### **Is the MicroBlaze FPU IEEE-754 compliant?**

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The MicroBlaze FPU is IEEE-754 compatible, but not fully compliant. It deviates from the standard in certain infrequent corner cases:

- An operation on a quiet NaN will return a fixed NaN, not one of the operands.
- Only round-to-nearest mode is supported.
- Denormalized operands are not supported. If exceptions are enabled, a denormal exception will be generated. Otherwise a quiet NaN will be returned.
- Denormalized results are flushed to zero.

If necessary these corner cases can be handled using software libraries called from exception handlers.

### **Can I reduce the size of the FPU by only selecting individual operations?**

No. The only configuration option supported for the FPU is whether FPU exceptions are used or not. Individual operations like fadd, fsub, etc. cannot be configured separately.

### **Do I need any special floating point libraries to use the FPU?**

No. The floating point operations are part of the MicroBlaze ISA and are automatically recognized by the compiler. Any operation on the C data type 'float' will be automatically inferred by the compiler to use the FPU.

### **Does the MicroBlaze core support user-defined instructions?**

User-defined instructions are fairly complex solutions to hardware acceleration. The MicroBlaze processor uses a more robust and versatile co-processor solution to achieve the same objective. The low latency Fast Simplex Link (FSL) can connect up to eight co-processors, each of which can naturally perform more than one custom function. A co-processor function can also go beyond the two operands and a single result that normally limits user-defined instructions. Finally, there is less risk of harming the processor maximum frequency with a co-processor since it is not part of the pipeline.

### **Does the MicroBlaze core have branch prediction?**

Branch prediction is employed on architecture with long pipelines in which branches are resolved late in the pipeline. In the MicroBlaze core, however, branches are resolved in the third stage. As a result, a taken branch can have at most a two cycle penalty. Even this two cycle penalty is reduced by the automatic use of branches with delay slot instructions by the compiler. Therefore, the MicroBlaze core has a zero cycle penalty on not taken branches, and a one cycle penalty on taken branches with a delay slot instruction.

### **What's new with the MicroBlaze core for EDK9.2?**

- Optional Memory Management Unit (MMU) or Memory Protection Unit (MPU)
- Interface to a higher performance bus infrastructure (PLB v4.6)
- 3<sup>rd</sup> party trace tools
- FPU enhancements (integer to FP convert; FP square root)
- EDK Makes Choosing the Processor Easier
  - Base System Builder automatically selects:
    - Size-optimized MicroBlaze core for Spartan
    - Performance-optimized MicroBlaze core for Virtex

### **Why a Performance-optimize (5-stage) or Size-optimized (3-stage) MicroBlaze core?**

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The MicroBlaze v7.00 is the latest MicroBlaze core (EDK 9.2). This core is configurable for performance-optimized (5-stage pipeline) or cost-focused (3-stage pipeline) applications. It is 100% binary backward compatible with previous MicroBlaze core releases. The additional pipeline stages in the performance-optimized mode help lower the clock per instruction (CPI) which improves the overall processor performance to 1.15 DMIPS/MHz. The MicroBlaze v7.00 is at its smallest core size when used with 3 pipeline stages. This is an ideal choice for cost-focused MicroBlaze Spartan applications.

### **Where can I get additional information on MicroBlaze?**

Visit [www.xilinx.com/microblaze](http://www.xilinx.com/microblaze) for more information.